Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	301376	integrated adj circuit	US-PGPUB; USPAT	OR	ON	2005/01/27 17:22
S2	19699	S1 and timer and state	US-PGPUB; USPAT	OR	ON	2005/01/27 14:52
S3	11723	S2 and activat$4	US-PGPUB; USPAT	OR	ON	2005/01/27 14:52
S4	6030	S3 and disabl$4	US-PGPUB; USPAT	OR	ON	2005/01/27 15:13
S5	45	S4 and piracy	US-PGPUB; USPAT	OR	ON	2005/01/27 15:14
S6	264	713/194.ccls.	US-PGPUB; USPAT	OR	ON	2005/01/28 09:08
S7	104	713/194.ccls. and integrated adj circuit	US-PGPUB; USPAT	OR	ON	2005/01/27 15:31
S8	129	713/194.ccls. and tamper	US-PGPUB; USPAT	OR	ON	2005/01/27 15:31
S9	195	713/194.ccls.	USPAT	OR	ON	2005/01/27 15:31
S10	4029	STMICROELECTRONICS.as.	US-PGPUB; USPAT	OR	ON	2005/01/27 15:38
S11	4029	STMICROELECTRONICS.as.	US-PGPUB; USPAT	OR	ON	2005/01/27 15:38
S12	2162	STMICROELECTRONICS.as. and integrated adj circuit	US-PGPUB; USPAT	OR	ON	2005/01/27 15:39
S13	1510	STMICROELECTRONICS.as. and integrated adj circuit	USPAT	OR	ON	2005/01/27 15:39
S14	48353	integrated adj circuit and MOS	US-PGPUB; USPAT	OR	ON	2005/01/27 17:22
S15	398	integrated adj circuit and MOS and "713"/$.ccls.	US-PGPUB; USPAT	OR	ON	2005/01/27 17:23
S16	103	713/194.ccls. and (integrated adj circuit) and (secur$4 or protect$4)	US-PGPUB; USPAT	OR	ON	2005/01/27 18:03
S17	19	713/194.ccls. and (integrated adj circuit) and (secur$4 or protect$4) and timer	US-PGPUB; USPAT	OR	ON	2005/01/27 18:09
S18	12452	processing adj sequence	US-PGPUB; USPAT	OR	ON	2005/01/27 18:09
S19	4068	processing adj sequence and semiconductor	US-PGPUB; USPAT	OR	ON	2005/01/27 18:10
S20	4756	processing adj sequence and (semiconductor or integrated adj circuit)	US-PGPUB; USPAT	OR	ON	2005/01/27 18:10
S21	370	processing adj sequence and (semiconductor or integrated adj circuit) and timer and (active$4 or disabl$4)	US-PGPUB; USPAT	OR	ON	2005/01/27 18:11
S22	372	processing adj sequence and (semiconductor or integrated adj circuit) and timer and (active$4 or disabl$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/01/27 18:14
S23	31	S22 and ("713"/$.ccls. or "380"/$.ccls.)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/01/27 18:15
S24	1	("2002/0124183").URPN.	USPAT	OR	ON	2005/01/27 18:16
S25	5	("20020124183" | "4109312" | "4879645" | "5550919" | "5640003").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2005/01/27 18:16
S26	0	("6726108").URPN.	USPAT	OR	ON	2005/01/27 18:17
S27	41754	integrated adj circuit.ab.	US-PGPUB; USPAT	OR	ON	2005/01/28 09:00
S28	631	integrated adj circuit.ab. and ("713"/$.ccls. or "380"/$.ccls.)	US-PGPUB; USPAT	OR	ON	2005/01/28 09:01

S29	0	integrated adj circuit.ab. and "timer.ab"	US-PGPUB; USPAT	OR	ON	2005/01/28 09:01
S30	139	integrated adj circuit.ab. and timer.ab.	US-PGPUB; USPAT	OR	ON	2005/01/28 09:03
S31	19848	(integrated adj circuit) same protect$3	US-PGPUB; USPAT	OR	ON	2005/01/28 09:04
S32	187	(integrated adj circuit) same protect$3 same timer	US-PGPUB; USPAT	OR	ON	2005/01/28 09:41
S33	36	713/194.ccls. and timer	US-PGPUB; USPAT	OR	ON	2005/01/28 09:12
S34	4	("5533727"|"6236197"|"6357007"|"6369719").PN.	US-PGPUB; USPAT	OR	ON	2005/01/28 09:12
S35	33	("4222068" | "4521852" | "4521853" | "4613901" | "4634808" | "4696034" | "4887296" | "5029207" | "5237610" | "5293424" | "5436621" | "5442704" | "5592552" | "5619247" | "5754647" | "5757919" | "5764762" | "5774546" | "5799080" | "5802274" | "5809140" | "5825878" | "5852290" | "5892899" | "5892900" | "5923759" | "5982899" | "5999623" | "6009177" | "6041412" | "6044155" | "6049608" | "6069957").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2005/01/28 09:18
S36	74	("5293424").URPN.	USPAT	OR	ON	2005/01/28 09:24
S37	0	(integrated adj circuit) and piracy and timer and (disabl$4 adj3 integrated adj circuit)	USPAT	OR	ON	2005/01/28 09:26
S38	1	(integrated adj circuit) and piracy and timer and (disabl$4 adj3 integrated adj circuit)	US-PGPUB; USPAT	OR	ON	2005/01/28 09:26
S39	81	(integrated adj circuit) and piracy and timer	US-PGPUB; USPAT	OR	ON	2005/01/28 09:27
S40	5	(integrated adj circuit) same piracy and timer	US-PGPUB; USPAT	OR	ON	2005/01/28 09:30
S41	1	"4985920".pn.	US-PGPUB; USPAT	OR	ON	2005/01/28 09:30
S42	187	(integrated adj circuit or smart adj card) same protect$3 same timer	US-PGPUB; USPAT	OR	ON	2005/01/28 09:42
S43	109	differential adj power adj analysis	US-PGPUB; USPAT	OR	ON	2005/01/28 09:47
S44	3102	(differential adj power adj analysis) or DPA	US-PGPUB; USPAT	OR	ON	2005/01/28 09:51
S45	145	((differential adj power adj analysis) or DPA) and timer	US-PGPUB; USPAT	OR	ON	2005/01/28 09:52
S46	29	((differential adj power adj analysis) or DPA) and timer and (integrated adj circuit or smart adj card)	US-PGPUB; USPAT	OR	ON	2005/01/28 09:52
S47	394047	integrated adj circuit or IC or smart adj card	US-PGPUB; USPAT	OR	ON	2005/01/31 14:00
S48	1476346	integrated adj circuit or IC or smart adj card	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/01/31 14:03
S49	10584	S48 and (tamper$8 or pirac$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/01/31 14:44
S50	9071	S49 and (time$4 or count$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/01/31 14:51
S51	14127	processing adj sequence	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/01/31 14:52

S52	148	S50 and S51	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/01/31 15:22
S53	29	integrated adj circuit same piracy	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/01/31 16:43
S54	7	"5981323".pn. "5943264".pn. "6225679".pn. "6362671".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/01/31 15:05
S55	4	"5981323".pn. "5943264".pn. "6225679".pn. "6362671".pn.	USPAT	OR	ON	2005/01/31 15:05
S56	14	("5867655"|"20030194094"|"20020186842"|"6289455"|"6219771"|"5559992"|"4584665").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/01/31 15:21
S57	4	("6233339"|"5917909").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/01/31 15:21
S58	57	simple adj power adj analysis or single adj power adj analysis	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/01/31 16:13
S59	4	("4327438").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/01/31 16:14
S60	8	("4932053"|"6304658").PN. ("4327438").PN. ("4932053"|"6304658").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/01/31 16:15
S61	8	("4932053"|"6304658").PN. ("4327438").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/01/31 16:26
S62	2	("5452358").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/01/31 16:29
S63	4	("4179657"|"6064740").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/01/31 16:30

S64	2	("5961578").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/01/31 16:30
S65	7	integrated adj circuit same piracy	USPAT	OR	ON	2005/01/31 16:44
S66	16	integrated adj circuit same piracy	US-PGPUB	OR	ON	2005/01/31 16:45
S67	38	(US-20010016910-$ or US-20010047480-$ or US-20010054163-$ or US-20020067198-$ or US-20020083283-$ or US-20020131596-$ or US-20020166058-$ or US-20020199111-$ or US-20030030417-$ or US-20030101351-$ or US-20030188170-$ or US-20030210018-$ or US-20030229597-$ or US-20040150382-$ or US-20040162993-$).did. or (US-4109312-$ or US-4179657-$ or US-4327438-$ or US-4879645-$ or US-4932053-$ or US-5469557-$ or US-5515540-$ or US-5550919-$ or US-5640003-$ or US-5961578-$ or US-6175951-$ or US-6289455-$ or US-6292898-$ or US-6298135-$ or US-6304658-$ or US-6357007-$ or US-6507913-$ or US-6696822-$ or US-6726108-$ or US-6757831-$).did. or (DE-2854832-$ or US-5452358-$ or EP-1282072-$).did.	US-PGPUB; USPAT; DERWENT	OR	ON	2005/02/01 06:20
S68	272	disabl$4 adj3 integrated adj circuit	US-PGPUB; USPAT	OR	ON	2005/02/01 06:45
S69	187	disabl$4 adj2 integrated adj circuit	US-PGPUB; USPAT	OR	ON	2005/02/01 06:45
S70	1	(disabl$4 adj3 integrated adj circuit) and (activa$4 adj2 timer) and (detect$4 adj3 (state or status))	US-PGPUB; USPAT	OR	ON	2005/02/01 06:46
S71	3503	protect$4 adj3 integrated adj circuit	US-PGPUB; USPAT	OR	ON	2005/02/01 06:47
S72	365	S71 and (timer or counter)	US-PGPUB; USPAT	OR	ON	2005/02/01 06:53
S73	301744	integrated adj circuit	US-PGPUB; USPAT	OR	ON	2005/02/01 06:53
S74	2097	S73 near4 timer	US-PGPUB; USPAT	OR	ON	2005/02/01 06:54
S75	904	S74 same (activat$4 or deactivat$4 or turn$4 or switch$4)	US-PGPUB; USPAT	OR	ON	2005/02/01 06:54
S76	98	S75 same detect$4	US-PGPUB; USPAT	OR	ON	2005/02/01 07:36
S77	15	"6362671".pn. "6225679".pn. "5943264".pn. "5981323".pn. ("4855690").PN. ("6573800"|"6070178"|"5412587"|"4176399"|"6571263"|"5961577"|"3790768").PN. ("6188294"|"5128998"|"4578649").PN.	US-PGPUB; USPAT	OR	ON	2005/02/01 07:15
S78	5559	(integrated adj circuit) same timer	US-PGPUB; USPAT	OR	ON	2005/02/01 07:37
S79	1636	(integrated adj circuit) same timer same power	US-PGPUB; USPAT	OR	ON	2005/02/01 07:37
S80	271	(integrated adj circuit) same timer and ("713"/$.ccls. or "380"/$.ccls.)	US-PGPUB; USPAT	OR	ON	2005/02/01 07:37
S81	222	(integrated adj circuit) same timer and ("713"/$.ccls. or "380"/$.ccls.)	USPAT	OR	ON	2005/02/01 08:10
S82	222	(integrated adj circuit) same timer and ("713"/$.ccls. or "380"/$.ccls.)	USPAT	OR	ON	2005/02/01 08:37
S83	33	S82 and operating.ab.	USPAT	OR	ON	2005/02/01 08:10
S84	168	(integrated adj circuit) same capacitor and ("713"/$.ccls. or "380"/$.ccls.)	USPAT	OR	ON	2005/02/01 08:40
S85	43	(integrated adj circuit) same capacitor and ("713"/$.ccls. or "380"/$.ccls.) and (discharge)	USPAT	OR	ON	2005/02/01 08:41
S86	4	(US-4317180-$ or US-4965828-$ or US-5563799-$ or US-6307480-$).did.	USPAT	OR	ON	2005/02/01 09:07
S87	125	(SPA or Single adj Power adj Analysis or Simple adj Power adj Analysis) and (DPA or Differential adj Power adj Analysis)	US-PGPUB; USPAT	OR	ON	2005/02/01 10:28

S88	124	S87 and tim$4	US-PGPUB; USPAT	OR	ON	2005/02/01 10:32
S89	23	S87 and tim$4 and capacitor	US-PGPUB; USPAT	OR	ON	2005/02/01 10:37
S97	7	("4742215" | "5065429" | "5513133" | "5519843" | "5544246" | "5742530" | "6249869").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2005/02/01 10:43
S98	14	(US-20020067198-$ or US-20020131596-$ or US-20040039928-$ or US-20040105541-$ or US-20040030905-$ or US-20010047480-$ or US-20010016910-$ or US-20040028234-$ or US-20040078588-$ or US-20040025032-$ or US-20030210018-$ or US-20030110390-$ or US-20020112156-$).did. or (US-6839849-$).did.	US-PGPUB; USPAT	OR	ON	2005/02/01 10:52
S99	3	"4799258".pn. "5546463".pn. "5848159".pn.	US-PGPUB; USPAT	OR	ON	2005/02/01 10:59
S100	2	("5249294"|"20020029346").PN.	US-PGPUB; USPAT	OR	ON	2005/02/01 11:01
S101	2	("5944833"|"5249294").PN.	US-PGPUB; USPAT	OR	ON	2005/02/01 11:05
S102	2	("5944833"|"5249294").PN. and (counter or tim$4)	US-PGPUB; USPAT	OR	ON	2005/02/01 11:05
S103	14	(US-20020067198-$ or US-20020131596-$ or US-20040039928-$ or US-20040105541-$ or US-20040030905-$ or US-20010047480-$ or US-20010016910-$ or US-20040028234-$ or US-20040078588-$ or US-20040025032-$ or US-20030210018-$ or US-20030110390-$ or US-20020112156-$).did. or (US-6839849-$).did.	US-PGPUB; USPAT	OR	ON	2005/02/01 11:11
S104	6	((US-20020067198-$ or US-20020131596-$ or US-20040039928-$ or US-20040105541-$ or US-20040030905-$ or US-20010047480-$ or US-20010016910-$ or US-20040028234-$ or US-20040078588-$ or US-20040025032-$ or US-20030210018-$ or US-20030110390-$ or US-20020112156-$).did. or (US-6839849-$).did.) and tim$4 and capacitor	US-PGPUB; USPAT	OR	ON	2005/02/01 11:19
S105	930	watch$1dog adj circuit or tempest$4 adj circuit	US-PGPUB; USPAT	OR	ON	2005/02/01 11:25
S106	5	("5949160" "5321752" "5664017" "5315257" "5448639").pn.	US-PGPUB; USPAT	OR	ON	2005/02/01 11:24
S107	292	(watch$1dog adj circuit or tempest$4 adj circuit) and integrated adj circuit	US-PGPUB; USPAT	OR	ON	2005/02/01 11:26
S108	215	(watch$1dog adj circuit or tempest$4 adj circuit) and integrated adj circuit	USPAT	OR	ON	2005/02/01 11:44
S109	4	("5944833" "5249294" "6236197" "6357007" "4317180" "4965828" "6307480" "5563799" "6507913" "6839849" "20010047480").pn. and timer and capacitor and integrated adj circuit	USPAT	OR	ON	2005/02/01 12:24
S110	4	("5944833" "5249294" "6236197" "6357007" "4317180" "4965828" "6307480" "5563799" "6507913" "6839849" "20010047480").pn. and timer and capacitor and integrated adj circuit	US-PGPUB; USPAT	OR	ON	2005/02/01 16:18
S111	10	(watch$1dog adj circuit or tempest$4 adj circuit) and integrated adj circuit and ("713"/$.ccls. or "380"/$.ccls.)	USPAT	OR	ON	2005/02/01 11:59
S112	1	"5815577".pn.	USPAT	OR	ON	2005/02/01 12:09
S121	8	("5944833" "5249294" "6236197" "6357007" "4317180" "4965828" "6307480" "5563799" "6507913" "6839849" "20010047480").pn. and timer	US-PGPUB; USPAT	OR	ON	2005/02/01 16:18
S122	0	("5944833" "5249294" "6236197" "6357007" "4317180" "4965828" "6307480" "5563799" "6507913" "6839849" "20010047480").pn. and (deactivat$4 adj4 timer)	US-PGPUB; USPAT	OR	ON	2005/02/01 16:18
S123	8	("5944833" "5249294" "6236197" "6357007" "4317180" "4965828" "6307480" "5563799" "6507913" "6839849" "20010047480").pn. and timer	US-PGPUB; USPAT	OR	ON	2005/02/01 16:22

S125	6	("5944833" "5249294" "6236197" "6357007" "4317180" "4965828" "6307480" "5563799" "6507913" "6839849" "20010047480").pn. and threshold	US-PGPUB; USPAT	OR	ON	2005/02/01 16:22
S126	3	("5944833" "5249294" "6236197" "6357007" "4317180" "4965828" "6307480" "5563799" "6507913" "6839849" "20010047480").pn. and threshold and counter	US-PGPUB; USPAT	OR	ON	2005/02/01 16:25
S127	3	("5944833" "5249294" "6236197" "6357007" "4317180" "4965828" "6307480" "5563799" "6507913" "6839849" "20010047480").pn. and threshold and counter and (non-volatile or nonvolatile or ROM)	US-PGPUB; USPAT	OR	ON	2005/02/01 16:35
S128	1	"4591782".pn.	US-PGPUB; USPAT	OR	ON	2005/02/01 16:29
S129	5	("5944833" "5249294" "6236197" "6357007" "4317180" "4965828" "6307480" "5563799" "6507913" "6839849" "20010047480").pn. and cpu	US-PGPUB; USPAT	OR	ON	2005/02/01 16:39
S130	10	("5944833" "5249294" "6236197" "6357007" "4317180" "4965828" "6307480" "5563799" "6507913" "6839849" "20010047480").pn. and (timer or counter)	US-PGPUB; USPAT	OR	ON	2005/02/01 16:38
S131	11	("5944833" "5249294" "6236197" "6357007" "4317180" "4965828" "6307480" "5563799" "6507913" "6839849" "20010047480").pn. and (cpu or process$3)	US-PGPUB; USPAT	OR	ON	2005/02/01 16:41
S132	6	("5944833" "5249294" "6236197" "6357007" "4317180" "4965828" "6307480" "5563799" "6507913" "6839849" "20010047480").pn. and (cpu or process$3) and protect$4 and (timer or counter)	US-PGPUB; USPAT	OR	ON	2005/02/02 08:12
S143	1	"2000003295".pran.	JPO	OR	ON	2005/02/02 07:58
S144	1	"2000003295".pran. "2000003297".pran. "2000323178".pran.	JPO	OR	ON	2005/02/02 07:59
S145	1	"2000003295".pran. or "2000003297".pran. or "2000323178". pran.	JPO	OR	ON	2005/02/02 07:59
S146	1	"2000003295".pran.	JPO	OR	ON	2005/02/02 07:59
S150	1	"5961578".pn.	USPAT; JPO	OR	ON	2005/02/02 08:02
S152	2	("4179657"|"6064740").PN.	USPAT; JPO	OR	ON	2005/02/02 08:03
S153	7	("5944833" "5249294" "6236197" "6357007" "4317180" "4965828" "6307480" "5563799" "6507913" "6839849" "20010047480").pn. and counter	US-PGPUB; USPAT	OR	ON	2005/02/02 08:40
S156	351734	("5944833" "5249294" "6236197" "6357007" "4317180" "4965828" "6307480" "5563799" "6507913" "6839849" "20010047480").pn. and counter adn threshold	US-PGPUB; USPAT	OR	ON	2005/02/02 08:37
S157	3	("5944833" "5249294" "6236197" "6357007" "4317180" "4965828" "6307480" "5563799" "6507913" "6839849" "20010047480").pn. and counter and threshold	US-PGPUB; USPAT	OR	ON	2005/02/02 08:37
S158	543	("380"/$.ccls. or "713"/$.ccls.) and counter and threshold and integrated adj circuit	US-PGPUB; USPAT	OR	ON	2005/02/02 08:38
S159	383	("380"/$.ccls. or "713"/$.ccls.) and counter and threshold and integrated adj circuit	USPAT	OR	ON	2005/02/02 08:38
S160	6	("380"/$.ccls. or "713"/$.ccls.) and counter same threshold same integrated adj circuit	USPAT	OR	ON	2005/02/02 08:38
S161	10	("5944833" "5249294" "6236197" "6357007" "4317180" "4965828" "6307480" "5563799" "6507913" "6839849" "20010047480").pn. and (counter or timer or loop)	US-PGPUB; USPAT	OR	ON	2005/02/02 08:40
S162	528619	(integrated adj circuit or smart adj card)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/02/02 08:46

S163	1476826	(integrated adj circuit or smart adj card or IC)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/02/02 10:43
S164	2	S163 and (counter same protect$4 adj area same (rom or read adj only adj memory or non$1volatile adj memory))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/02/02 08:50
S165	11344	S163 and (counter same (rom or read adj only adj memory or non$1volatile adj memory))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/02/02 08:50
S166	302	S163 and (counter same protect$4 same (rom or read adj only adj memory or non$1volatile adj memory))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/02/02 08:51
S167	26	S166 and ("713"/$.ccls. or "380"/$.ccls.)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/02/02 08:51
S168	17	(US-20010016910-$ or US-20010047480-$ or US-20020067198-$ or US-20020112156-$ or US-20020131596-$ or US-20030110390-$ or US-20030210018-$ or US-20040025032-$ or US-20040028234-$ or US-20040030905-$ or US-20040039928-$ or US-20040078588-$ or US-20040105541-$).did. or (US-6839849-$ or US-6553496-$ or US-5497462-$ or US-5657444-$).did.	US-PGPUB; USPAT	OR	ON	2005/02/02 08:59
S169	4	(US-6839849-$ or US-6553496-$ or US-5497462-$ or US-5657444-$).did.	USPAT	OR	ON	2005/02/02 09:00
S170	3	S167 and S169	US-PGPUB; USPAT	OR	ON	2005/02/02 09:07
S171	3	S170 and counter	US-PGPUB; USPAT	OR	ON	2005/02/02 09:15
S172	3	S170 and protect$4	US-PGPUB; USPAT	OR	ON	2005/02/02 09:23
S173	1	"6292898".pn.	US-PGPUB; USPAT	OR	ON	2005/02/02 09:55
S174	339	erase$4 same data same (intrusion or tamper$4)	US-PGPUB; USPAT	OR	ON	2005/02/02 09:56
S175	184	erase$4 same data same (intrusion or tamper$4)	USPAT	OR	ON	2005/02/02 10:28
S180	511984	integrated adj circuit	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/02/02 10:30
S181	528619	integrated adj circuit or smart adj card	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/02/02 10:30

S182	1476826	integrated adj circuit or smart adj card or ic	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/02/02 10:30
S183	45183	S182 and timer$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/02/02 10:31
S184	1697	S183 and authenticat$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/02/02 10:31
S185	1627	S184 and (state or power$6 or switch$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/02/02 10:32
S186	329	S185 and ("713"/$.ccls. or "380"/$.ccls.)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/02/02 10:32
S187	153	S185 and ("713"/$.ccls. or "380"/$.ccls.)	USPAT	OR	ON	2005/02/02 10:36
S188	706	watchdog adj circuit	USPAT	OR	ON	2005/02/02 10:36
S189	454	S188 and timers	USPAT	OR	ON	2005/02/02 10:42
S190	13	S189 and authenticat$4	USPAT	OR	ON	2005/02/02 10:36
S191	454	S188 and timer$4	USPAT	OR	ON	2005/02/02 10:38
S192	13	S188 and timer$4 and authenticat$4	USPAT	OR	ON	2005/02/02 10:40
S198	475	S188 and (timer$3 or time$1out)	USPAT	OR	ON	2005/02/02 10:42
S199	13	S188 and (timer$3 or time$1out) and authenticat$4	USPAT	OR	ON	2005/02/02 10:43
S200	12938	(integrated adj circuit or smart adj card or IC) and (timeout or time-out or time adj out)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/02/02 10:44
S201	1064	(integrated adj circuit or smart adj card or IC) and (timeout or time-out or time adj out) and authentication	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/02/02 10:44
S202	247	(integrated adj circuit or smart adj card or IC) and (timeout or time-out or time adj out) and authentication and ("713"/$.ccls. or "380"/$.ccls.)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/02/02 10:44
S203	105	(integrated adj circuit or smart adj card or IC) and (timeout or time-out or time adj out) and authentication and ("713"/$.ccls. or "380"/$.ccls.)	USPAT	OR	ON	2005/02/02 11:16

S204	230	authenticat$4 same timer	USPAT	OR	ON	2005/02/02 11:16
S205	0	S204 same integrated adj circuit	USPAT	OR	ON	2005/02/02 11:17
S206	4	S204 same (integrated adj circuit or smart adj card)	USPAT	OR	ON	2005/02/02 11:20
S210	1813	detect$3 adj power adj supply	US-PGPUB; USPAT	OR	ON	2005/02/02 17:20
S211	9642	detect$4 adj4 power adj suppl$3	US-PGPUB; USPAT	OR	ON	2005/02/03 07:55
S212	2381	S211 and integrated adj circuit	US-PGPUB; USPAT	OR	ON	2005/02/03 07:56
S213	632	S212 and timer	US-PGPUB; USPAT	OR	ON	2005/02/03 07:56
S214	971	S212 and (timer or counter)	US-PGPUB; USPAT	OR	ON	2005/02/03 07:56
S215	122	S214 and (piracy or tamper$4)	US-PGPUB; USPAT	OR	ON	2005/02/03 07:56
S216	571	S214 and (piracy or tamper$4 or protect$4)	US-PGPUB; USPAT	OR	ON	2005/02/03 07:57
S217	12608	timer adj circuit	US-PGPUB; USPAT	OR	ON	2005/02/03 07:57
S218	3637	S217 and integrated adj circuit	US-PGPUB; USPAT	OR	ON	2005/02/03 07:57
S219	7	S215 and S218	US-PGPUB; USPAT	OR	ON	2005/02/03 07:57
S220	4	(US-5497462-$ or US-5657444-$ or US-6553496-$ or US-6839849-$).did.	USPAT	OR	ON	2005/02/03 08:06
S221	302925	integrated adj circuit	US-PGPUB; USPAT	OR	ON	2005/02/09 08:28
S222	313075	integrated adj circuit or smart adj card	US-PGPUB; USPAT	OR	ON	2005/02/09 08:28
S223	38045	piracy or tamper$4	US-PGPUB; USPAT	OR	ON	2005/02/09 08:28
S224	5607	S222 and S223	US-PGPUB; USPAT	OR	ON	2005/02/09 08:29
S225	30200	"713"/$.ccls. or "380"/$.ccls.	US-PGPUB; USPAT	OR	ON	2005/02/09 08:33
S226	1750	S224 and S225	US-PGPUB; USPAT	OR	ON	2005/02/09 08:29
S227	195560	"713"/$.ccls. or "380"/$.ccls. or "257"/$.ccls.	US-PGPUB; USPAT	OR	ON	2005/02/09 08:34
S228	1828	S227 and S224	US-PGPUB; USPAT	OR	ON	2005/02/09 08:35
S229	1168	S228 and power$6	US-PGPUB; USPAT	OR	ON	2005/02/09 08:35
S230	514	S229 and (timer or counter)	US-PGPUB; USPAT	OR	ON	2005/02/09 08:36
S231	632	S229 and (timer or counter or timing)	US-PGPUB; USPAT	OR	ON	2005/02/09 08:36
S232	388	S229 and (timer or counter or timing)	USPAT	OR	ON	2005/02/09 08:38
S233	296	S232 and (integrated adj circuit)	USPAT	OR	ON	2005/02/09 08:54
S236	35	tempest and ("713"/$.ccls. or "380"/$.ccls.)	US-PGPUB; USPAT	OR	ON	2005/02/09 09:14
S243	265	713/194.ccls.	US-PGPUB; USPAT	OR	ON	2005/02/09 09:18
S244	104	713/194.ccls. and (integrated adj circuit)	US-PGPUB; USPAT	OR	ON	2005/02/09 09:26
S245	13	marinet.in.	US-PGPUB; USPAT	OR	ON	2005/02/09 09:29

S246	460	(integrated adj circuit) and piracy	US-PGPUB; USPAT	OR	ON	2005/02/09 09:29
S247	151	(integrated adj circuit) and piracy and (timer or counter)	US-PGPUB; USPAT	OR	ON	2005/02/09 09:30
S248	86	(integrated adj circuit) and piracy and (timer or counter)	USPAT	OR	ON	2005/02/09 09:30
S249	19354	motorola.as.	US-PGPUB; USPAT	OR	ON	2005/02/09 10:19
S250	5959	motorola.as. and integrated adj circuit	US-PGPUB; USPAT	OR	ON	2005/02/09 10:20
S251	135	motorola.as. and integrated adj circuit and ("713"/$.ccls. or "380"/$.ccls.)	US-PGPUB; USPAT	OR	ON	2005/02/09 10:20
S252	0	motorola.as. and integrated adj circuit and ("713"/$.ccls. or "380"/$.ccls.) and piracy	US-PGPUB; USPAT	OR	ON	2005/02/09 10:20
S253	248	integrated adj circuit and ("713"/$.ccls. or "380"/$.ccls.) and piracy	US-PGPUB; USPAT	OR	ON	2005/02/09 10:21
S254	108	integrated adj circuit and ("713"/$.ccls. or "380"/$.ccls.) and piracy and (timer or counter)	US-PGPUB; USPAT	OR	ON	2005/02/09 12:58
S255	108	integrated adj circuit and ("713"/$.ccls. or "380"/$.ccls.) and piracy and (timer or counter)	US-PGPUB; USPAT	OR	ON	2005/02/09 13:11
S256	0	integrated adj circuit and piracy and (timer or counter)	JPO	OR	ON	2005/02/09 13:11
S257	0	integrated adj circuit and piracy and (timer or counter)	EPO	OR	ON	2005/02/09 13:12
S258	11053	integrated adj circuit	EPO	OR	ON	2005/02/09 13:12
S263	55311	integrated adj circuit	JPO	OR	ON	2005/02/09 14:07
S266	968	S263 and module	JPO	OR	ON	2005/02/09 13:14
S267	264	S263 and timer	JPO	OR	ON	2005/02/09 14:06
S268	1	S267 and ("713"/$.ccls.)	JPO	OR	ON	2005/02/09 14:05
S269	1	S267 and ("713"/$.ccls. or "380"/$.ccls.)	JPO	OR	ON	2005/02/09 14:05
S270	8	S267 and ("714"/$.ccls. or "380"/$.ccls.)	JPO	OR	ON	2005/02/09 14:05
S271	0	S263 and timer	EPO	OR	ON	2005/02/09 14:06
S272	11053	integrated adj circuit	EPO	OR	ON	2005/02/09 14:07
S273	54	S272 and timer	EPO	OR	ON	2005/02/09 14:07
S277	1557	activat$4 same timer same power adj supply	US-PGPUB; USPAT	OR	ON	2005/02/09 14:32
S278	1557	activat$4 same timer same (power adj supply)	US-PGPUB; USPAT	OR	ON	2005/02/09 14:32
S279	346	S278 and integrated adj circuit	US-PGPUB; USPAT	OR	ON	2005/02/09 14:46
S280	23	("4317180"|"4965828"|"4882752"|"6292898"|"5469557"|"5880523"|"5159629"|"6839849"|"6625741"|"6507913"|"6236197"|"5249294"|"20020067198"|"20010047480"|"6357007"|"6307480"|"5944833"|"5563799"|"6246970"|"4924513"|"4881263"|"5027397"|"4811288").PN.	US-PGPUB; USPAT	OR	ON	2005/02/09 14:47
S281	20	S280 and power	US-PGPUB; USPAT	OR	ON	2005/02/09 14:47
S282	18	S281 and supply	US-PGPUB; USPAT	OR	ON	2005/02/09 14:49
S283	15	S280 and power adj supply	US-PGPUB; USPAT	OR	ON	2005/02/09 14:49

S284	3155975	S283 nd tim$4	US-PGPUB; USPAT	OR	ON	2005/02/09 14:49
S285	15	S283 and tim$4	US-PGPUB; USPAT	OR	ON	2005/02/09 14:54
S293	10640	MOS same transistor same bipolar	US-PGPUB; USPAT	OR	ON	2005/02/09 15:54
S294	1365	MOS same transistor same bipolar same capacitor	US-PGPUB; USPAT	OR	ON	2005/02/09 15:54
S295	35	S293 and ("713"/$.ccls. or "380"/$.ccls.)	US-PGPUB; USPAT	OR	ON	2005/02/09 15:55
S298	12057	test adj circuit	US-PGPUB; USPAT	OR	ON	2005/02/11 07:37
S299	120	test adj circuit and ("713"/$.ccls. or "380"/$.ccls.)	US-PGPUB; USPAT	OR	ON	2005/02/11 08:01
S300	40	test adj circuit and ("713"/1$.ccls. or "380"/$.ccls.)	US-PGPUB; USPAT	OR	ON	2005/02/11 07:50
S301	22	test adj circuit and ("713"/1$.ccls.)	US-PGPUB; USPAT	OR	ON	2005/02/11 07:50
S302	15	test adj circuit and ("713"/1$.ccls.)	USPAT	OR	ON	2005/02/11 07:55
S303	23273	discharg$3 adj capacitor	USPAT	OR	ON	2005/02/11 07:56
S304	92	test adj circuit and ("713"/$.ccls. or "380"/$.ccls.)	USPAT	OR	ON	2005/02/11 08:07
S305	20	test adj circuit and ("713"/194.ccls. or "380"/$.ccls.)	USPAT	OR	ON	2005/02/11 08:12
S308	3	"6839849".pn. "5497462".pn. "6292898".pn.	USPAT	OR	ON	2005/02/11 08:10
S309	2	S308 and test$4	USPAT	OR	ON	2005/02/11 08:10
S313	25	test adj circuit and ("713"/194.ccls. or "380"/$.ccls.)	US-PGPUB; USPAT	OR	ON	2005/02/11 08:12
S314	10	("5638306" | "5828824" | "6065106" | "6072328" | "6081885" | "6118296" | "6184048" | "6331784" | "6466048" | "6472902").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2005/02/11 08:14
S315	10	("5638306" | "5828824" | "6065106" | "6072328" | "6081885" | "6118296" | "6184048" | "6331784" | "6466048" | "6472902").PN. and test$4	US-PGPUB; USPAT; USOCR	OR	ON	2005/02/11 08:19
S316	306708	integrated adj circuit	US-PGPUB; USPAT; USOCR	OR	ON	2005/02/11 08:19
S317	11106	S316 and test$4 adj (circuit or procedure)	US-PGPUB; USPAT; USOCR	OR	ON	2005/02/11 08:20
S318	1208	S317 and timer	US-PGPUB; USPAT; USOCR	OR	ON	2005/02/11 08:20
S319	999	S317 and timer	USPAT	OR	ON	2005/02/11 08:20
S320	1208	S317 and timer	US-PGPUB; USPAT; USOCR	OR	ON	2005/02/11 08:21
S321	44	S317 and timer and ("713"/$.ccls. or "380"/$.ccls)	US-PGPUB; USPAT; USOCR	OR	ON	2005/02/11 08:21
S322	50	S317 and timer and ("713"/$.ccls. or "380"/$.ccls.)	US-PGPUB; USPAT; USOCR	OR	ON	2005/02/11 08:21
S326	25743	discharg$4 adj capacitor	US-PGPUB; USPAT	OR	ON	2005/02/11 08:37
S327	2170	S326 same (faster or rapidly or quicker)	US-PGPUB; USPAT	OR	ON	2005/02/11 08:37

S328	7	S327 and ("713"/$.ccls. or "380"/$.ccls.)	US-PGPUB; USPAT	OR	ON	2005/02/11 08:53
S329	31129	capacitor same discharg$4 same control$4	US-PGPUB; USPAT	OR	ON	2005/02/11 08:54
S330	170	S329 and ("713"/$.ccls. or "380"/$.ccls.)	US-PGPUB; USPAT	OR	ON	2005/02/11 08:54

Terms used **integrated circuit timer capacitor** Found **13** of **150,138**

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Relevance scale

1 Converting a 64b PowerPC processor from CMOS bulk to SOI technology
D. Allen, D. Behrends, B. Stanisic
June 1999 **Proceedings of the 36th ACM/IEEE conference on Design automation**
Full text available: pdf(90.91 KB) Additional Information: full citation, references, citings, index terms

2 System-level power optimization: techniques and tools
Luca Benini, Giovanni de Micheli
April 2000 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 5 Issue 2
Full text available: pdf(385.22 KB) Additional Information: full citation, abstract, references, citings, index terms

This tutorial surveys design methods for energy-efficient system-level design. We consider electronic sytems consisting of a hardware platform and software layers. We consider the three major constituents of hardware that consume energy, namely computation, communication, and storage units, and we review methods of reducing their energy consumption. We also study models for analyzing the energy cost of software, and methods for energy-efficient software design and compilation. This survery ...

3 Mixed-signal design and simulation: A 16-bit mixed-signal microsystem with integrated CMOS-MEMS clock reference
Robert M. Senger, Eric D. Marsman, Michael S. McCorquodale, Fadi H. Gebara, Keith L. Kraver, Matthew R. Guthaus, Richard B. Brown
June 2003 **Proceedings of the 40th conference on Design automation**
Full text available: pdf(793.60 KB) Additional Information: full citation, abstract, references, citings, index terms

In this work, we report on an unprecedented design where digital, analog, and MEMS technologies are combined to realize a general-purpose single-chip CMOS microsystem. The convergence of these technologies has enabled the development of a low power, portable microinstrument ideally suited for controlling environmental and bio-implantable sensors.

Keywords: ADC, MEMS, PGA, SD, SoC, clock generation, design methodology, inductor, low power, low voltage analog, microcontroller, microsystem, mixed-signal, system-on-chip, varactor

4 Low-power micromachined microsystems (invited talk)
Khalil Najafi
August 2000 **Proceedings of the 2000 international symposium on Low power**

electronics and design

Full text available: pdf(1.40 MB) Additional Information: full citation, abstract, references, index terms

Micromachined microsystems and Micro Electro Mechanical Systems (MEMS) have made possible the development of highly accurate and portable sensors and instrument for a variety of applications in the health care, industrial, consumer products, avionics, and defense. Design of low-power circuits for these applications, and use of micromachined sensors and actuators in combination with integrated circuits to implement even lower power microinstruments has now become possible and the focus of at ...

Keywords: MEMS, energy harvesting, low-power, micromachining, microsystems, power sources

5 A static power model for architects

J. Adam Butts, Gurindar S. Sohi

December 2000 **Proceedings of the 33rd annual ACM/IEEE international symposium on Microarchitecture**

Full text available: pdf(136.88 KB) ps(431.76 KB) Publisher Site Additional Information: full citation, references, citings, index terms

6 Optimization techniques for high-performance digital circuits

Chandu Visweswariah

November 1997 **Proceedings of the 1997 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(190.24 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

The relentless push for high performance in custom digital circuits has led to renewed emphasis on circuit optimization or tuning. The parameters of the optimization are typically transistor and interconnect sizes. The design metrics are not just delay, transition times, power and area, but also signal integrity and manufacturability. This tutorial paper discusses some of the recently proposed methods of circuit optimization, with an emphasis on practical application and methodology impact. Circ ...

Keywords: nonlinear optimization, circuit tuning, gradients, adjoints

7 Opportunities and obstacles in low-power system-level CAD

Andrew Wolfe

June 1996 **Proceedings of the 33rd annual conference on Design automation**

Full text available: pdf(73.19 KB) Additional Information: full citation, references, citings, index terms

8 Teaching digital logic design using a tape recorder simulator

R. P. Srivastava

February 1990 **Proceedings of the 1990 ACM SIGSMALL/PC symposium on Small systems**

Full text available: pdf(658.62 KB) Additional Information: full citation, abstract, references, index terms

This paper describes two implementations of a tape recorder simulator. One is based on hard-wired logic and the other on microcomputer programmed logic approach. Both implementations are compared and evaluated for such points as flexibility, speed, power and space requirements, and cost. The purpose of this paper is to introduce students of digital logic design to the problems of selecting a suitable implementation based on software and hardware requirements, and system constraints. This is ...

9 BIST and production testing of ADCs using imprecise stimulus

Kumar Parthasarathy, Turker Kuyel, Dana Price, Le Jin, Degang Chen, Randall Geiger

October 2003 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 8 Issue 4

Full text available: pdf(500.33 KB) Additional Information: full citation, abstract, references, index terms

A new approach for testing mixed-signal circuits based upon using imprecise stimuli is introduced. Unlike most existing Built-In Self-Test (BIST) and production test approaches that require excitation signals that are at least 3 bits or more linear than the Device-Under-Test (DUT), the proposed approach can work with stimuli that are several bits less linear than the DUT. This dramatically reduces the requirements on stimulus generation for BIST applications and offers potential for using inexpe ...

Keywords: ADC linearity, Analog and mixed-signal testing, built-in self-test, imprecision measurement, imprecision stimulus, production test

10 Achieving simulation-based test program verification and fault simulation capabilities for mixed-signal systems

P. Caunegre, C. Abraham

March 1995 **Proceedings of the 1995 European conference on Design and Test**

Full text available: pdf(901.13 KB) Publisher Site Additional Information: full citation, abstract

A simulation-based methodology for test program verification is presented. Executing test programs on a virtual test system allows simulation of Device Under Test (DUT) behavior. Simulating both device and test hardware and software allows test engineers to check and debug test programs without fabricated devices. It results in a gain of time and permits design and test to occur concurrently. This also yields better overall circuit testability. Our effort concerns development of Automatic Testin ...

Keywords: Automatic Testing Equipment, Device Under Test, automatic test software, circuit analysis computing, circuit testability, design, fault diagnosis, fault simulation, hardware, integrated circuit testing, mixed analogue-digital integrated circuits, mixed-signal systems, program debugging, program verification, software interfaces, test program verification, virtual test system

11 Global harmony: coupled noise analysis for full-chip RC interconnect networks

K. L. Shepard, V. Narayanan, P. C. Elmendorf, Gutuan Zheng

November 1997 **Proceedings of the 1997 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(238.78 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

Noise is becoming one of the most important metrics in the design of VLSI systems, certainly of comparable importance to area, timing, and power. In this paper, we describe Global Harmony, a methodology for the analysis of coupling noise in the global interconnect of large VLSI chips, being developed for the design of high-performance microprocessors. The architecture of Global Harmony involves a careful combination of static noise analysis, static timing analysis, and reduced-order modelling te ...

Keywords: noise, static timing analysis, interconnect

12 Highlights of ISSCC and the design of state-of-the-art microprocessors: Physical synthesis methodology for high performance microprocessors

Yiu-Hing Chan, Prabhakar Kudva, Lisa Lacey, Greg Northrop, Thomas Rosser

June 2003 **Proceedings of the 40th conference on Design automation**

Full text available: pdf(461.05 KB) Additional Information: full citation, abstract, references, citings, index terms

Integrated logic synthesis and physical design (physical synthesis) continues to play a very important role in high performance microprocessor design methodologies. In this paper, we present the integrated physical synthesis timing closure methodology used in the current generation microprocessors. Physical synthesis techniques were aggressively used as part of logic and placement optimizations for performance, power and area. The design turn around times were significantly reduced and timing co ...

Keywords: high-performance, microprocessors, synthesis

13 The Chinook hardware/software co-synthesis system

Pai H. Chou, Ross B. Ortega, Gaetano Borriello

September 1995 **Proceedings of the 8th international symposium on System synthesis**

Full text available: pdf(79.55 KB) Additional Information: full citation, abstract, references, citings, index terms

Publisher Site

Abstract: Designers of embedded systems are facing ever tighter constraints on design time, but computer-aided design tools for embedded systems have not kept pace with these trends. The Chinook co-synthesis system addresses the automation of the most time-consuming and error-prone tasks in embedded controller design, namely the synthesis of interface hardware and software needed to integrate system components, the migration of functions between processors or custom logic, and the co-simulation ...

Keywords: Chinook hardware/software co-synthesis system, computer-aided design tools, custom logic, design co-simulation, design time constraints, embedded controller design, error-prone tasks, function migration, interface hardware, interface software, logic CAD, logic design, microcontrollers, microprocessors, real-time systems, software tools, system components integration

Results 1 - 13 of 13